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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/659,235	09/11/2000	William O'Leary	100.136US01	4655

7590 03/18/2004

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EXAMINER	
BUTLER, DENNIS	
ART UNIT	**PAPER NUMBER**
2115	5

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/659,235	O'LEARY, WILLIAM	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25,32,42 and 45-63* is/are allowed.

6)☒ Claim(s) *1-24,26-31,33-41,43,44 and 64-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to amendment A received on January 6, 2004. Claims 1-66 are pending. Claims 46-66 have been added.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. The drawings are objected to because they do not show all of the claimed features including a phase detector that is a two-state phase detector that uses XOR logic, a phase detector that is a two-state phase detector that is a sequential phase detector and a phase detector that is a three-state phase detector as recited in the claims. Element 212 of figure does not show the above limitations as stated by applicant. Element 212 of figure 2 is merely a box labeled Phase Detector and fails to show the above claimed embodiments. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. Claims 1-5, 10-14, 19-22, 26-31, 43-44 and 64-66 are rejected under 35 U.S.C. 102(b) as being anticipated by McCauley, U. S. Patent 4,847,678.

Per claims 1, 10, 26, 31, 43 and 64-66:

A) McCauley teaches the following claimed items:

1. a phase detector generating an error signal (phase sign) with Phase detector 48 of figure 2 and at column 5, lines 1-25;

2. a digital counter receiving the error signal (phase sign) and a sampling clock signal (phase error) and generating a count value indicating the amount of

phase error with Up/Down Counter 52 of figure 2, at column 5, lines 12-25 and 56-61, with figure 7 and at column 7, lines 47-62;

3. a digital to analog converter converting the count value to an error voltage with D/A converter 62 of figures 2 and 8, at column 5, lines 56-61 and at column 7, line 63 – column 8, line 1;

4. a filter that filters the error voltage with the low pass filter including op amp 131 and the attached resistors and capacitor in figure 8 and at column 8, lines 1-11;

5. a voltage controlled oscillator with VCO 34 of figures 2 and 8, at column 5, lines 56-61 and at column 8, lines 12-56.

Per claims 2-5, 11-14 and 27:

McCauley teaches a sequential two-state phase detector that has XOR logic with the circuit comprising XOR gate 102 and the phase error output of figure 3. McCauley teaches a three-state phase detector with the circuit comprising XOR gate 102, XOR gate 82, the phase error output and the phase sign output of figure 3.

Per claim 19:

McCauley teaches the filter comprising an active filter with the low pass filter including op amp 131 and the attached resistors and capacitor in figure 8 and at column 8, lines 1-11.

Per claims 20-22, 29 and 30:

McCauley teaches that the voltage controlled oscillator (VCO) is a crystal oscillator and outputs a feedback signal to a frequency divider with crystal 132 of figure 8, divider 64 of figure 2 at column 5, lines 56-68 and at column 8, lines 12-56.

Per claims 28 and 44:

McCauley teaches incrementing the digital counter in response to a sampling clock (phase error signal), setting the counter to àn initial value, incrementing in response to phase lead and decrementing in response to phase lag with figures 2 and 7, at column 5, lines 12-25 and 56-61, at column 6, lines 36-41 and at column 7, lines 47-62.

5. Claims 6-9, 15-18, 23-24 and 33-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCauley, U. S. Patent 4,847,678 in view of Takeuchi, U. S. Patent 5,727,193.

Claims 23-24 seem to differ from McCauley in that McCauley fails to explicitly teach providing a frequency divider for dividing the reference signal and inputting the divided reference signal into the phase detector as claimed. However, Takeuchi describes that it is known to provide a frequency divider for dividing the reference signal and inputting the divided reference signal into the phase detector with frequency divider 27 of figure 2 at column 3, line 43 – column 4, line 9. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a frequency divider for dividing the reference signal and inputting the divided reference signal into the phase

detector, as taught by Takeuchi, in order to increase the flexibility of the phase detecting and locking circuitry by allowing a greater number of possible reference signals and/or frequencies to be applied to the system and provide the ability to generate a fractional speed clock signal. One of ordinary skill in the art would have been motivated to combine McCauley and Takeuchi because of Takeuchi's suggestion at column 4, lines 45-51. It would have been obvious for one of ordinary skill in the art to combine McCauley and Takeuchi because they are both directed to the problem of generating a signal that is synchronized to a reference signal using a phase locked loop. Claims 33 and 40 are similar in scope and content to claims 10, 11, 19, 22 and 23 and are rejected for the same reasons as these claims. Claims 34-39 and 41 are similar in scope and content to claims 12, 13, 15, 20, 22 and 24 and are rejected for the same reasons as these claims. Claims 6-9 and 15-18 recite obvious variations of well known timing and synchronization procedures and circuitry and would have been obvious in view of the teachings and suggestions of McCauley and Takeuchi. Applicant's claims 6-9 and 15-18 are directed to matching components and clock frequency so that they are compatible with each other. McCauley teaches a counter with a sampling clock input that is directly connected to a digital to analog converter that samples the digital count value of the counter and produces an analog signal for the VCO with figure 2. It would clearly be obvious to use compatible or matched counter and D/A components and signals in order to increase the reliability and reduce the cost of the timing system.

6. Claims 25, 32, 42, 45 and 46-63 are allowable over the art of record because the art of record does not teach or suggest the combination of recited elements.

7. Applicant's arguments filed on January 6, 2004 have been fully considered but they are not persuasive.

In the Remarks, applicant has argued in substance that:

A. The term "sampling clock signal" carries with it the meaning that it is a clock signal that is used to gather a plurality of values during a given sampling period. Applicant provides a definition for "sampling" and argues that McCauley does not teach sampling and/or a sampling clock.

B. McCauley provides exactly one pulse during the measurement window. Therefore, the phase error signal is not a sampling clock.

C. In McCauley, each event results in incrementing or decrementing the counter once. The amount by which the counter is incremented is not related to the amount of phase difference and the count value is not indicative of the amount of phase error during a single event.

D. McCauley does not show a sampling clock and does not show incrementing a counter in response to a sampling clock during the time an error signal has a first logic state.

E. Applicant traverses the statement that claims 6-9 and 15-18 recite obvious variations of well known timing and synchronization procedures and circuitry and would have been obvious in view of the teachings and suggestions of McCauley

and Takeuchi and the examiner must provide a reference and citation to bach-up this assertion in the next action.

8. As to point A, the examiner disagrees with applicant's contentions. McCauley clearly teaches the claimed sampling clock. Regarding applicant's definition of sampling, the element that applicant has directed this definition to recites a digital counter that provides a count value. Webster's Dictionary defines a counter as an electronic or mechanical device that automatically counts occurrences or repetitions of phenomena or events. A counter is not defined as a sampling device as defined by applicant. A counter is specifically designed to count (increment or decrement) occurrences or events and not merely produce a set of discrete values. Therefore, applicant's sampling definition does not apply to the recited counter. Regarding the sampling clock signal, McCauley describes a digital counter having a second input for receiving a sampling clock signal with the CLK input of up/down counter 52 of figure 2. McCauley describes that when counter 52 is clocked its value changes once, either up or down depending on the value of the phase sign signal input to the UP/DN input at column 7, lines 21-24. Therefore, McCauley describes that the value at the UP/DN input of counter 52 is sampled using the clock signal input to the CLK input. McCauley clearly teaches a digital counter having a second input for receiving a sampling clock signal as claimed.

As to point B, it is unclear how applicant's arguments relate to the claimed invention. The claims do not recite a measurement window. Therefore, it is irrelevant whether McCauley discloses providing exactly one pulse during the measurement

window. McCauley describes a digital counter having a second input for receiving a sampling clock signal with the CLK input of up/down counter 52 of figure 2. McCauley describes that when counter 52 is clocked its value changes once, either up or down depending on the value of the phase sign signal input to the UP/DN input at column 7, lines 21-24. Therefore, McCauley describes that the value at the UP/DN input of counter 52 is sampled using the clock signal input to the CLK input. McCauley clearly teaches a digital counter having a second input for receiving a sampling clock signal as claimed.

As to point C, the examiner disagrees with applicant's contentions. Applicant's seem to assume that McCauley's PLL is not designed properly and would not be able to properly lock on to the phase of the reference clock as designed. McCauley's PLL circuit was clearly designed with a fine enough resolution to lock on to the phase of the reference clock and track any phase change to the reference clock during a synchronization event. See column 2, line 50 – column 3, line 2. McCauley describes incrementing the counter in relation to the amount of phase difference by incrementing the count value up or down based on the phase difference measurement of the phase detector. McCauley describes that the count value is indicative of the amount of phase error during a single event (synchronization event) at column 5, lines 1-25. McCauley teaches the invention to the extent claimed.

As to point D, the examiner disagrees with applicant's contentions. McCauley clearly teaches the claimed sampling clock as described in the response to point A. McCauley describes incrementing a counter in response to a sampling clock during the

time an error signal has a first logic state at column 6, lines 36-41 and at column 7, lines 21-24.

As to point E, the examiner is not required to provide applicant a reference or a citation because the applied references provide both motivation and suggestion to modify McCauley's timing system in view of the knowledge generally available to one of ordinary skill in the art. Applicant's claims 6-9 and 15-18 are directed to matching components and clock frequency so that they are compatible with each other. McCauley teaches a counter with a sampling clock input that is directly connected to a digital to analog converter that samples the digital count value of the counter and produces an analog signal for the VCO with figure 2. It would clearly be obvious to use compatible or matched counter and D/A components and signals in order to increase the reliability and reduce the cost of the timing system.

9. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Dennis M. Butler
Primary Examiner
Art Unit 2115